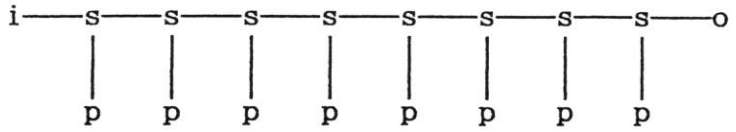
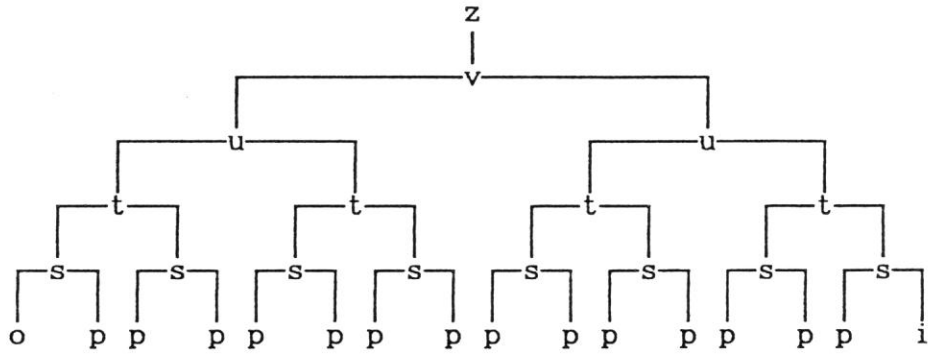
2. ABOUT TREE STRUCTURES...

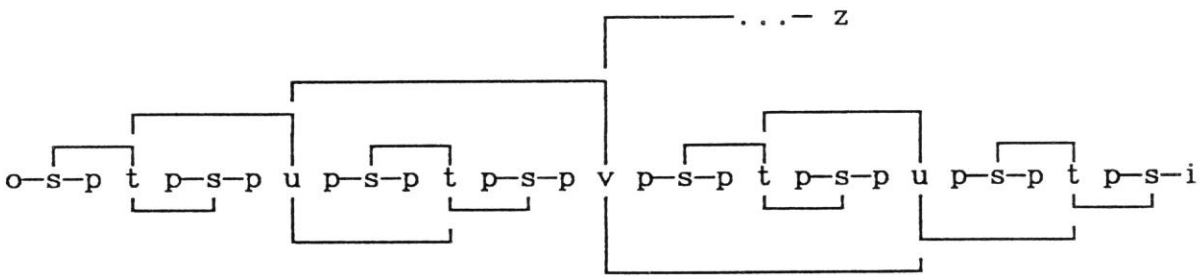
LINEARIZED TREES



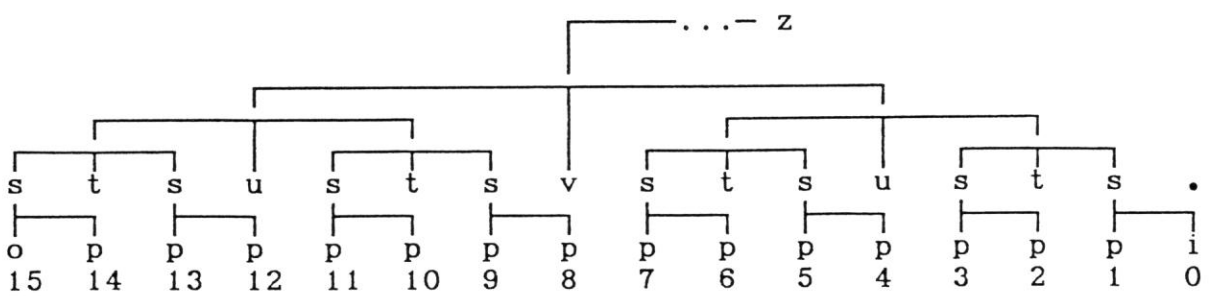
RIPPLE- ARRANGEMENT



BINARY TREE ARRANGEMENT



ONE ROW LINEARIZED, BINARY TREE

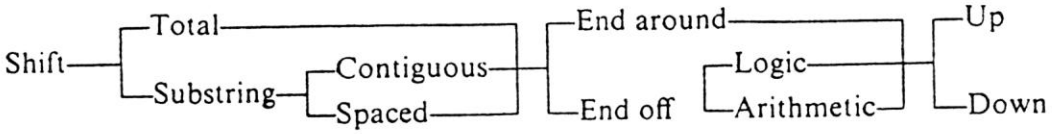


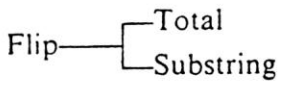
TWO ROWS LINEARIZED, BINARY TREE

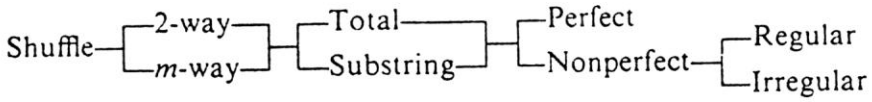
DATA MANIPULATING FUNCTIONS

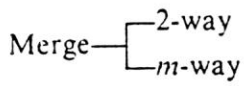
(Feng)

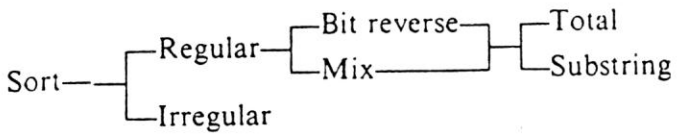
PERMUTING



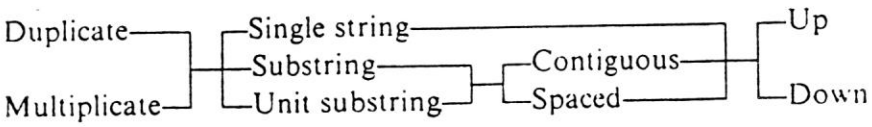




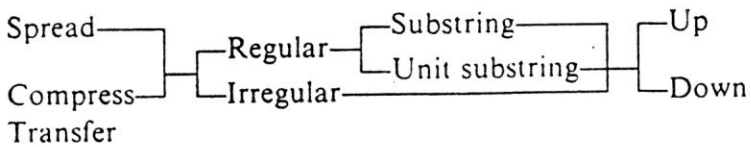




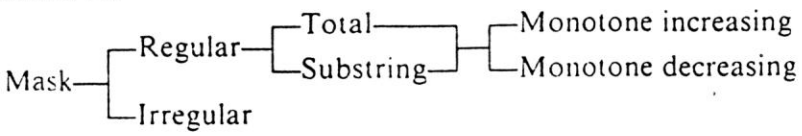
REPLICATING



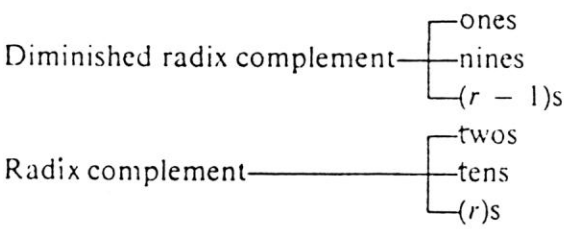
SPACING



MASKING



COMPLEMENTING



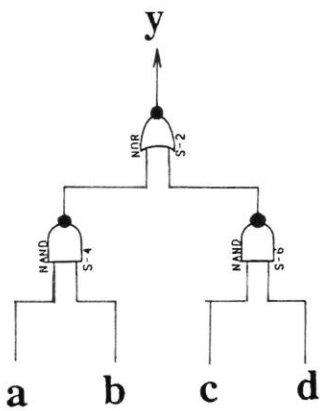
BOOLEAN SERIES

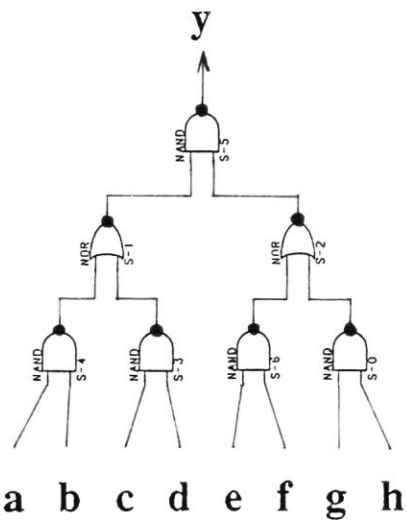
Problem: Only inverting (AOI-) gates are available to realize large gates with more than 4 inputs

GATE TREES

TREE HEIGHT

EVEN ← → ODD





$y = \overline{\overline{ab} \vee \overline{cd}}$

$y = \overline{\overline{a} \vee \overline{b} \vee \overline{c} \vee \overline{d}}$

$y = abcd$

$y = \overline{\overline{\overline{ab} \vee \overline{cd}} \;\&\; \overline{\overline{ef} \vee \overline{gh}}}$

$y = \overline{\overline{a} \vee \overline{b} \vee \overline{c} \vee \overline{d} \;\&\; \overline{e} \vee \overline{f} \vee \overline{g} \vee \overline{h}}$

$y = \overline{abcdefgh}$

APPLICATION

Zeroflag as generalized n- input OR / NOR / AND / NAND

COMPOSITION RULES

- logical function equals that of the tree root gates
- tree height: { even: not negated output; odd: negated output

HEIGHT_OF_TREE

$$\text{tree\_height} = \text{int}\,(\log_{\text{fanout}}(\text{buswidth}))$$

BINARY TREES:

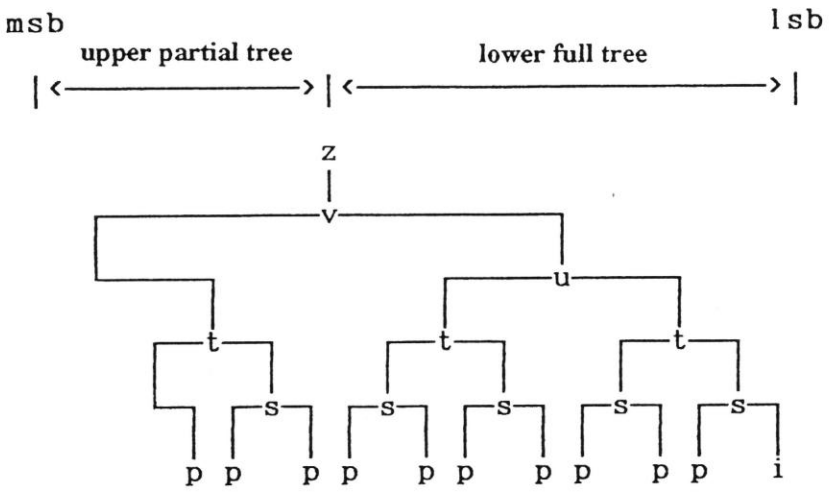
$$\text{tree\_height} = \text{int}\,(\text{ld}\,(\text{buswidth}))$$

(for partial trees too)

ROOT_OF_TREE POSITION

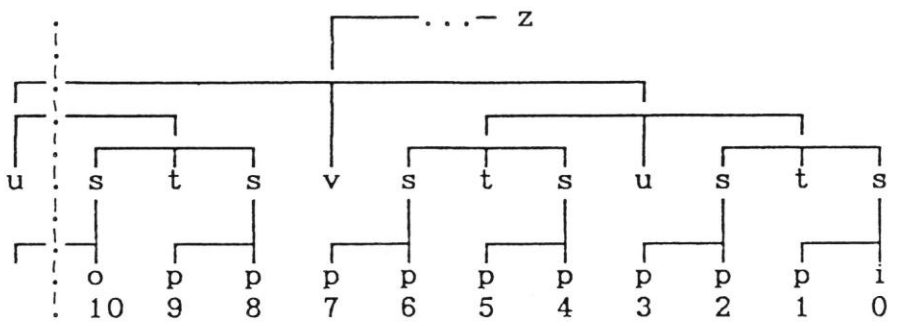
$$\text{root\_of\_tree} = \text{int}\left(\frac{\text{buswidth} - 1}{2}\right)$$

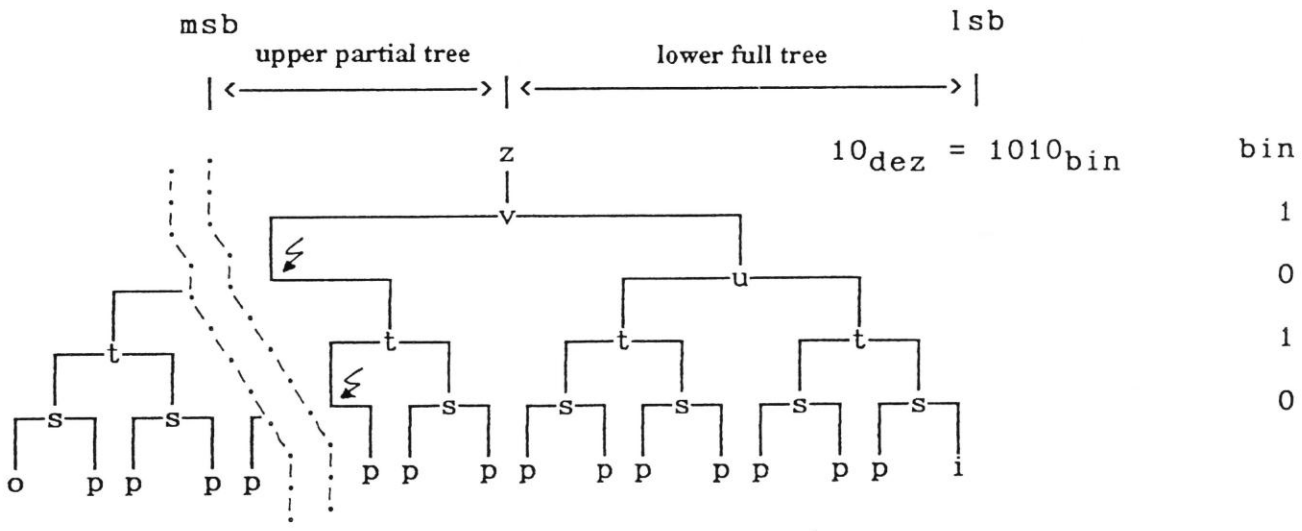
$$= \text{int}\left(\frac{\text{highest\_bit}}{2}\right)$$



CUTTING A TREE

GENERATING TREES WITH VARIABLE BUSWIDTH :
CUTTING A SWITCH (left most switch u)





Switches (u, s) are closed at Zero Positions

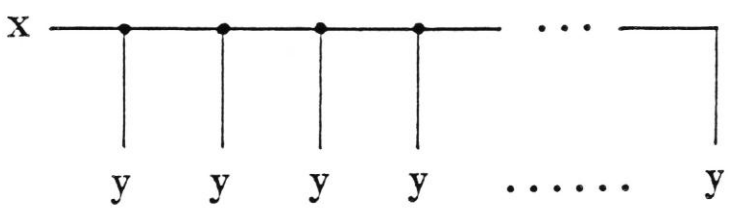
BUFFER TREES (WIRES)

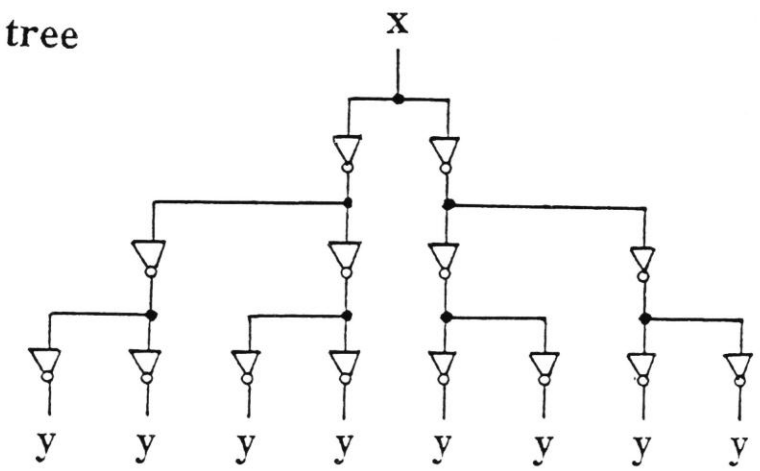
Problem:

wire fanout increases with buswidth -> bad timing!
e.g. CNTLs, CLOCK, RESET

Solution: compose trees!

y = x
:
= ~(~(~(...~(~(~x))...))) (even number of negations ~)

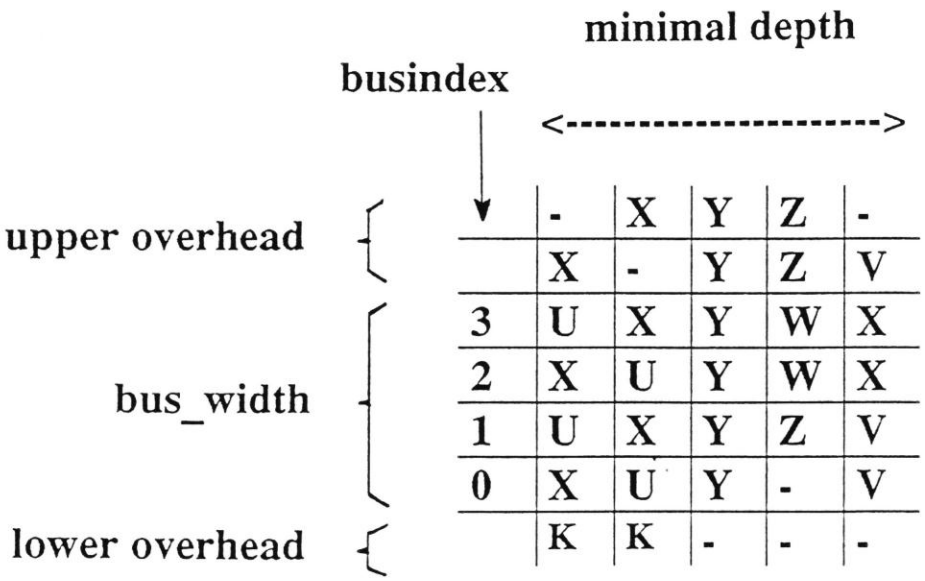


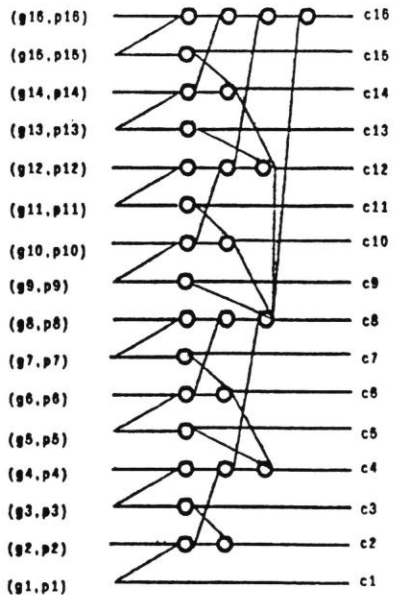


tree_height = log fanout (buswidth)

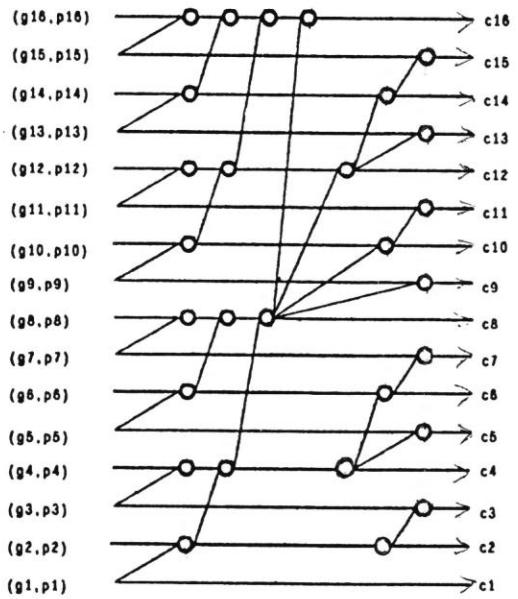
MATRIX FILLING

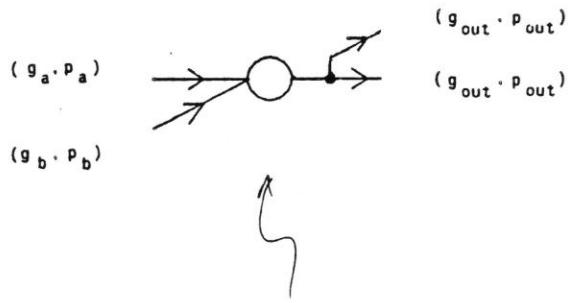
Strategy: Try to fill the matrix with minimum number of lacks
to minimize the width,
try to minimize the upper/ lower overhead;
arrange one tree into a closed column.





CARRY LOOKAHEAD ADDER: FOLDED TREE REPRESENTATION





$$g_{out} = g_a \vee (p_a \wedge g_b)$$

$$p_{out} = p_a \wedge p_b$$

CARRY LOOKAHEAD ADDER: INTERNAL CELL AND TREE STRUCTURE FOR CARRY GENERATION